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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,765	10/12/2001	Paul R. Gentieu	9775-0042-999	2095

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	5

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/976,765	Applicant(s) GENTIEU ET AL.	
	Examiner Eric Coleman	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-23,25-39 and 41-45* is/are rejected.

7)☒ Claim(s) *11,24 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10,12-23,25-30,38-39,41-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bakke (patent No. 5,566,170) in view of Stone (patent No. 5,598,410).

3. Bakke taught the invention substantially as claimed including a data processing ("DP") system comprising:

A) Processor (e.g., see fig.2);

B) Execution control unit (108) for executing instructions (e.g., see fig. 2);

C) Input pipeline unit (102) operable to receive input data words (140) (e.g., see fig. 2);

D) Data modify unit (126) coupled to the input pipeline unit (e.g., see fig. 2), the data modify unit operable to selectively modify input data words received from the input data pipeline according to instruction-specified operators to generate modified data words (e.g., see col. 9, line 55-col. 10, line 43 and col. 11, lines 18-40);

E) Processor output selector (110) operative to selectively output and instruction-specified one of the input data words and the modified data words (104) (e.g., see fig.2 and col. 9, lines 21-col. 10, line 36 and col. 11, line 1- col. 12, line 29).

4. Bakke did not expressly detail (claim 1,12,13,25,41) that synchronization of the system elements with the instruction clock. Stone however taught synchronization of the data protocol unit with the corresponding directive (e.g., see fig. 7 and col. 13, lines 20-51) generated by the processing unit preprocessor wherein plural data units can be interleaved during a particular time span (e.g., see col. 11, lines 1-col. 12,line 25). From the above clearly the system of Bakke and Stone would have been synchronized with directives (or commands or instructions) for modification of the data units. Since Stone taught the processor comprising an FPGA with a 40ns cycle time that provided data rate of 400-500 mega bits per second, clocking the processor would have provided an efficient properly timed system for controlling the generation of directives and processing the data units then one of ordinary skill would have been motivated to clock the processor (e.g., see col. 22, lines 36-45). With the processor clocked, the production of the directive would have been generated in a manner timed in relation to the processor clock, and consequently the synchronization of the data units by directives would have been synchronized by the instruction clock.

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings Bakke and Stone. First of all, Bakke expressly indicated that the Stone application (now patent) (serial number 08/366225) was related to the Bakke system (e.g., see col. 1, lines 5-20 of Bakke). Also, Incorporation of the Stone teachings of use of more than one preprocessor in a synchronized manner (e.g., see fig. 3) would have allowed the combined system to process an increased number of data units in a period of time.

6. As per claims 2,12,15,17,25,26 Bakke taught data compare unit (128) coupled to the input pipeline unit (e.g., see fig. 2) and generate compare flags (e.g., see col. 11, line 48-col. 12, line 14). As to the prediction of the next instruction depending of on the compare flags determined in a current cycle this type of branch prediction was well known in the DP art at the time of the claimed invention. One of ordinary skill would have been motivated use the branch history of at least the previous instruction to more efficiently execute the succeeding instruction as execution could have begun before next of the determination of the branch outcome had finished.

7. As per claim 14, Bakke taught data modify unit (126) coupled to the input pipeline unit (e.g., see fig. 2), the data modify unit operable to selectively modify input data words received from the input data pipeline according to instruction-specified operators to generate modified data words (e.g., see col. 9, line 55-col. 10, line 43 and col. 11, lines 18-40).

8. As per claim 42,43, Bakke taught the processing including interconnection performed in real-time (e.g., see col. 10, lines 6-25). As per claim 44 Stone taught a instruction memory (206)(e.g., see fig. 5)

9. As per claim 3,16, Bakke taught configuring the modify or compare unit each cycle of the instruction or directive to perform a specified operation on a data unit according to the current directive or instruction (e.g., see col. 11, lines 1-62).

10. As per claim 5,7,18,19,27,28,29,31, Bakke taught the input pipeline unit comprising successive stages each having an output, each respective stage operable to output a respective one of the input data words after a delay of a number of cycles of

the instruction clock signal corresponding to a position of the respective stage in the input pipeline unit (e.g., see fig. 2 and col. 9, lines 21-54) and output multiplexer means (120) coupled to at least a subset of the stages of the input pipeline unit, the output multiplexer operable to select for output to the data modifying unit and the data compare unit an instruction-specified one of the outputs for the subset of the stages of the input pipeline unit (e.g., see fig 2, and col. 9, lines 29-54).

11. As per claim 6,20,30,44 Stone taught register stack (208) (e.g., see fig. 5) accessible by the execution unit (214), data compare unit (236) and data modify unit; and peripheral accessible by the data modify unit, the peripheral unit (122,204) for storing instruction-specified data therein and instruction memory (206)(e.g., see figs. 2,5).

12. As per claim 8,21,32,33 Stone taught a data modify unit comprising an arithmetic logic unit (ALU) (e.g., see fig. 5).

13. As per claims 4,9,10,22,23,38,39 Bakke taught a system the performed operations depending of conditions of compared data. Therefore it would have been obvious to one of ordinary skill that the Stone directives or instructions were conditionally executed for different types of modification or no modification of data units each instruction cycle (e.g., see col. 11, lines 1-47). Further as to plural branch operators flags and determinations, Bakke taught performing a second branching determination if the first branching determination resulted in the a protocol type greater than 1500 for a data unit (e.g., see col. 11, lines 1-47).

14. Claims 31-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bakke in view of Stone as applied to claim 1-10,12-23,25-30,38-39,41-44 above, and further in view of Hardwick (patent No. 5,550,816).

15. Hardwick taught a plurality of input multiplexers and a plurality of output multiplexers a plurality of decision mechanisms and forwarding processors for input data units (e.g., see fig. 2) that operated in as parallel pipelines.

16. It would have been obvious to one of ordinary skill in the DP art at the time of the claimed invention to combine the teachings of Bakke and Hardwick. Bakke taught that the Hardwick application (and now patent) (serial number 08/366,227, method and apparatus for virtual switching) was related to the Bakke application (and now patent) (e.g., see col. 1, lines 5-20 of Bakke). Also the addition of the Hardwick teaching of parallel pipelines for performing the modification of the data and selective input and output of the data in a parallel manner in plural pipelines would have provided for increased throughput of data over the pipeline of Bakke. Therefore one of ordinary skill would have been motivated to incorporated the teachings of Hardwick at least to increase the throughput of the system for processing data units.

17. As per claim 32,33 Stone taught a data modify unit comprising an arithmetic logic unit (ALU) (e.g., see fig. 5).

18. As per claim 34,35 Bakke taught the input pipeline unit comprising successive stages each having an output, each respective stage operable to output a respective one of the input data words after a delay of a number of cycles of the instruction clock signal corresponding to a position of the respective stage in the input pipeline unit (e.g.,

see fig. 2 and col. 9, lines 21-54) and output multiplexer means (120) coupled to at least a subset of the stages of the input pipeline unit, the output multiplexer operable to select for output to the data modifying unit and the data compare unit an instruction-specified one of the outputs for the subset of the stages of the input pipeline unit (e.g., see fig 2, and col. 9, lines 29-54).

19. As per claim 36 Bakke taught a system the performed operations depending of conditions of compared data. Therefore it would have been obvious to one of ordinary skill that the Stone directives or instructions were conditionally executed for different types of modification or no modification of data units each instruction cycle (e.g., see col. 11, lines 1-47). Further as to plural branch operators flags and determinations, Bakke taught performing a second branching determination if the first branching determination resulted in the a protocol type greater than 1500 for a data unit (e.g., see col. 11, lines 1-47).

20. Claim 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bakke (patent No. 5,566,170) in view of Hardwick (patent No. 5,550,816).

21. Bakke taught the invention substantially as claimed including a data processing ("DP") system comprising:

A) Processor (e.g., see fig.2);

B) Execution control unit (108) for executing instructions (e.g., see fig. 2);

C) Input pipeline unit (102) operable to receive input data words (140) (e.g., see fig. 2);

D) Data modify unit (126) coupled to the input pipeline unit (e.g., see fig. 2), the data modify unit operable to selectively modify input data words received from the input data pipeline according to instruction-specified operators to generate modified data words (e.g., see col. 9, line 55-col. 10, line 43 and col. 11, lines 18-40);

E) Processor output selector (110) operative to selectively output and instruction-specified one of the input data words and the modified data words (104) (e.g., see fig.2 and col. 9, lines 21-col. 10, line 36 and col. 11, line 1- col. 12, line 29).

22. Bakke did not specify plurality of input mutiplexers or selectors, or plurality of output multiplexers of selectors. Hardwick however, taught a plurality of input multiplexers and a plurality of output multiplexers a plurality of decision mechanisms and forwarding processors for input data units (e.g., see fig. 2) that operated in as parallel pipelines.

23. It would have been obvious to one of ordinary skill in the DP art at the time of the claimed invention to combine the teachings of Bakke and Hardwick. Bakke taught that the Hardwick application (and now patent) (serial number 08/366,227, method and apparatus for virtual switching) was related to the Bakke application (and now patent) (e.g., see col. 1, lines 5-20 of Bakke). Also the addition of the Hardwick teaching of parallel pipelines for performing the modification of the data and selective input and output of the data in a parallel manner in plural pipelines would have provided for increased throughput of data over the pipeline of Bakke. Therefore one of ordinary skill would have been motivated to incorporated the teachings of Hardwick at least to increase the throughput of the system for processing data units.

24. Further, as per claim 45, Bakke taught the processing including interconnection performed in real-time (e.g., see col. 10, lines 6-25).

Allowable Subject Matter

25. Claims 11,24,40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wilford (patent No. 6,157,641) disclosed a multi-protocol packet recognition and switching system (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER

February 25, 2004